PATENT ABSTRACTS OF JAPAN

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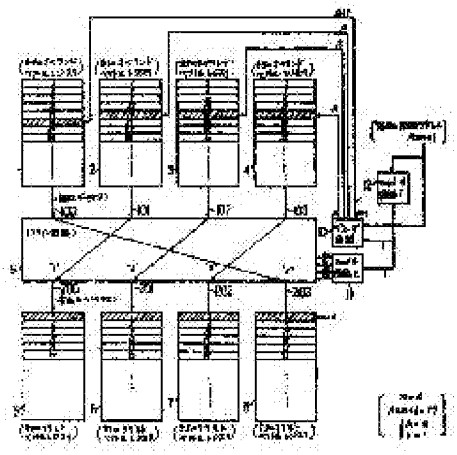
(54) **VECTOR PROCESSING DEVICE**



(57)Abstract:

PURPOSE: To execute a vector arithmetic at high speed by shifting a vector element in parallel from the (n) number of the operand vector registers to the (n) number of the result vector registers,.

CONSTITUTION: The outputs of the zeroWthe third operand vector registers 1W4 are inputted through respective data buses 100W103 to an aligning circuit 9. Further,the output data selectively rearranged in the aligning circuit 9 are connected through respective writing data buses 200W203 to the zeroWthe third result vector registers 5W8. A reading starting addresses (A×n+i) designated to operand vector registers 1W4 are inputted to the first mod 4 circuit 12, output a divided remainder (i) and are distributed to the second mod 4 circuit 11 and a decoder circuit 10. At the mod 4 circuit 11, 0+i, 1+i, 2+i and 3+i are respectively divided by (n), remainders l0, l1, l2 and l3 are respectively to the aligning circuit 9 as selecting signals and a decoder circuit 9 supplies A.